WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each including a capacitor having first and second electrodes, and a switching device having a control terminal connected to a corresponding word line among the plurality of word lines, and a current channel connected between the first electrode and a corresponding bit line among the plurality of bit lines,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, and the current channel of the switching device is set in a direction vertical to the semiconductor substrate.

2. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each including a capacitor having first and second electrodes, and a switching device having a control terminal connected to a corresponding word line among the plurality of word lines, and a current channel connected between the

first electrode and a corresponding bit line among the plurality of bit lines,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, and no leakage current channels are present between the switching device and the semiconductor substrate.

3. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each including a capacitor having first and second electrodes, and a switching device having a control terminal connected to a corresponding word line among the plurality of word lines, and a current channel connected between the first electrode and a corresponding bit line among the plurality of bit lines,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, and the switching device and the semiconductor substrate are insulated from each other by an insulating material.

4. A semiconductor apparatus according to claim

1, wherein the first mode is a normal mode for enabling a writing/reading operation to be executed in each of the memory cells, the first potential is a ground potential of a circuit, the second mode is a data holding mode for executing no writing/reading in the memory cell, and the second potential is a negative voltage lower than the ground potential of the circuit.

5. A semiconductor apparatus according to claim 1, wherein the first mode is a normal mode for enabling a writing/reading operation to be executed in each of the memory cells, the first potential is a first negative voltage lower than a ground potential of a circuit, the second mode is a data holding mode for executing no writing/reading in the memory cell, and the second potential is a second negative voltage lower than the first negative voltage.

6. A semiconductor apparatus according to claim 4, wherein each of the memory cells includes a PLED transistor, and a capacitor, and a refreshing operation is executed corresponding to respective data holding times of the first and second modes.

7. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of memory cells, each including a capacitor having first and second electrodes for holding an information voltage, a MOSFET having the information voltage of the capacitor supplied to a gate, and a writing transistor for supplying the

information voltage to the capacitor;

a plurality of word lines connected to the second electrode of the capacitor, and a gate of the writing transistor; and

a plurality of bit lines disposed in a direction orthogonal to the word lines for receiving a writing voltage and a source output of the MOSFET,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, when the semiconductor apparatus is on the first and second modes, an ON voltage of the word lines is set to be a third voltage for turning OFF the writing transistor when a signal corresponding to the information voltage is read, and turning ON the MOSFET when the information voltage of the capacitor is at a high level, and to be a fourth voltage for turning ON the writing transistor when a writing voltage is supplied from the bit lines to the capacitor, and a current channel of the writing transistor is set in a direction vertical to the semiconductor substrate.

8. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of memory cells, each including a capacitor having first and second electrodes for holding an information voltage, a MOSFET having the

information voltage of the capacitor supplied to a gate, and a writing transistor for supplying the information voltage to the capacitor;

a plurality of word lines connected to the second electrode of the capacitor, and a gate of the writing transistor; and

a plurality of bit lines disposed in a direction orthogonal to the word lines for receiving a writing voltage and a source output of the MOSFET,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, when the semiconductor apparatus is on the first and second modes, an ON voltage of the word lines is set to be a third voltage for turning OFF the writing transistor when a signal corresponding to the information voltage is read to the bit lines, and turning ON the MOSFET when the information voltage of the capacitor is at a high level, and to be a fourth voltage for turning ON the writing transistor when a writing voltage is supplied from the bit lines to the capacitor, and no leakage current channels are present between the writing transistor and the semiconductor substrate.

9. A semiconductor apparatus comprising on one semiconductor substrate:

a plurality of memory cells, each including a

capacitor having first and second electrodes for holding an information voltage, a MOSFET having the information voltage of the capacitor supplied to a gate, and a writing transistor for supplying the information voltage to the capacitor;

a plurality of word lines connected to the second electrode of the capacitor, and a gate of the writing transistor; and

a plurality of bit lines disposed in a direction orthogonal to the word lines for receiving a writing voltage and a source output of the MOSFET,

wherein when the semiconductor apparatus is on a first mode, an OFF potential of the word lines is set to be a first potential, when the semiconductor apparatus is on a second mode, an OFF potential of the word lines is set to be a second potential, when the semiconductor apparatus is on the first and second modes, an ON voltage of the word lines is set to be a third voltage for turning OFF the writing transistor when a signal corresponding to the information voltage is read to the bit lines, and turning ON the MOSFET when the information voltage of the capacitor is at a high level, and to be a fourth voltage for turning ON the writing transistor when a writing voltage is supplied from the bit lines to the capacitor, and the writing transistor and the semiconductor substrate are insulated from each other by an insulating material.

10. A semiconductor apparatus according to claim

7, wherein the first mode is a normal mode for enabling a writing/reading operation to be executed in each of the memory cells, the first potential is a ground potential of a circuit, the second mode is a data holding mode for executing no writing/reading in the memory cell, and the second potential is a negative voltage lower than the ground potential of the circuit.

11. A semiconductor apparatus according to claim 7, wherein the first mode is a normal mode for enabling a writing/reading operation to be executed in each of the memory cells, the first potential is a first negative voltage lower than a ground potential of a circuit, the second mode is a data holding mode for executing no writing/reading in the memory cell, and the second potential is a second negative voltage lower than the first negative voltage.

12. A semiconductor apparatus according to claim 10, wherein each of the memory cells includes a PLED transistor, and a capacitor, and a refreshing operation is executed corresponding to respective data holding times of the first and second modes.